REMARKS

This application has been reviewed in light of the Office Action dated February 4, 2005. Claims 1-11 and 18-34 are pending in this application. Claims 1, 18, 22, 26-28, and 32-34, all of which are independent claims, have been amended to define still more clearly what Applicant regards as his invention. Favorable reconsideration is requested.

The Office Action rejected Claims 1-11 and 18-31 under 35 U.S.C. § 103(a) as being obvious from U.S. Patent No. 5,838,678 (Davis et al.) in view of U.S. Patent 6,262,990 (Ejiri). Applicant respectfully traverses this rejection.

Applicant submits that independent Claims 1, 18, 22, 26-28, and 32-34, together with the remaining claims dependent therefrom, are patentable over the cited references for at least the following reasons.

It is believed that the general nature of the invention has been adequately discussed in previous papers, and that discussion will not be repeated.

Claim 1 is directed to an information processing apparatus that includes input means for inputting variable length packet data including packet length information indicative of a packet length and encoded information data, and judgment means for judging the packet length of the variable length packet data. Packet generating means generates the variable length packet data into fixed length packet data in accordance with an output of the judgment means, and transmits the fixed length packet data. The packet generating means includes memory means for generating fixed length data and initializing means for initializing the memory means by writing stuffing data in the memory means. The packet generating means generates the fixed length data by writing the variable length

packet data into the initialized memory means in accordance with the packet length judged by the judgment means and reads out the data from the memory means. In addition, the packet generating means generates the fixed length packet data in which the stuffing data is written, in case that the variable length packet data to be written into the memory means is shorter than a predetermined length.

Among other notable features of Claim 1 are that an information processing apparatus is arranged so that (1) packet generating means includes memory means for generating fixed length data and initializing means for initializing the memory means by writing stuffing data in the memory means (see, e.g., step S203 of the present application), (2) the packet generating means generates the fixed length data by writing variable length packet data into the initialized memory means in accordance with a judged packet length and reading out the data from the memory means, and (3) the packet generating means generates the fixed length packet data in which the stuffing data is written, in the case that the variable length packet data to be written into the memory means is shorter than a predetermined length.

Davis et al., as understood by Applicant, relates to pre-processing streams of encoded data to facilitate decoding streams back to back. In Fig. 9, cited in the Office Action, private data packets are inserted into buffer memory 932 before, after, or within pre-processed transport stream file(s) 940 (see, e.g., col. 10, lines 30-38).

The Office Action concedes, at page 4, that Davis et al. "does not teach the packet generating means generates the fixed length packet data to which the stuffing data is added, in case that the variable length packet data to be written into the memory means is

shorter than a predetermine[d] length." The Office cites Ejiri as allegedly teaching that feature.

Ejiri, as understood by Applicant, relates to a transmission system which multiplexes a plurality of data of different rates into a fixed length packet to be transmitted. More specifically, Ejiri discusses periodically generating a release timing signal which is in inverse proportion to the rate, to transmit data stored in a buffer memory as the fixed length packet data. According to this structure, Ejiri purports to avoid increased delay caused by the time required to store the burst data of an amount of payload of the fixed length packet in a buffer memory to generate the packet, and also purports to avoid delay caused by the time difference between the generated packet and the head of the next packet when the rearmost part of the burst data is packeted along with the head of the subsequent burst data.

In Ejiri, since the fixed length packet is released at the timing of the release timing signal regardless of whether or not the buffer memory is filled with the burst data, stuffing data is added into the fixed length packet (see, e.g., column 5, lines 34-41 and 50-53). However, Ejiri fails to teach or suggest initializing the buffer memory by writing stuffing data thereinto before generating the fixed length packet, and therefore does not teach or suggest the packet generating means recited in Claim 1.

Nothing in Davis et al. or Ejiri, whether considered separately or in any permissible combination (if any), would teach or suggest packet generating means which (1) includes memory means for generating fixed length data and initializing means for initializing the memory means by writing stuffing data in the memory means, (2) generates the fixed length data by writing variable length packet data into the initialized memory means in accordance with a judged packet length and reading out the data from the

memory means, and (3) generates the fixed length packet data in which the stuffing data is written, in the case that the variable length packet data to be written into the memory means is shorter than a predetermined length, as recited in Claim 1.

Accordingly, Applicant submits that Claim 1 is patentable over Davis et al. and Ejiri, whether considered separately or in any permissible combination (if any).

Independent Claims 26 and 32 recite features similar in many relevant respects to those discussed above with respect to Claim 1 and therefore are also believed to be patentable over Davis et al. and Ejiri for at least the reasons discussed above.

Claim 18 is directed to an information processing apparatus that includes first generating means for generating variable length packet data including encoded information data, second generating means for generating and transmitting first fixed length packet data from the generated variable length packet data, and generating means for generating clock reference information for use in a time reference during decoding of the encoded information data. The second generating means generates second fixed length packet data including the clock reference information and transmits the second fixed length packet data within a predetermined time interval, and compulsorily transmits the second fixed length packet data regardless of the predetermined time interval if there is no effective first fixed length packet data.

Among other notable features of Claim 18 are that an information processing apparatus is arranged so as to (1) generate clock reference information for use in a time reference during decoding of encoded information, (2) generate second fixed length packet data including the clock reference information to transmit the second fixed length packet data within a predetermined time interval, and (3) compulsorily transmit the second

fixed length packet data regardless of the predetermined time interval if there is no effective first fixed length packet data.

The Office Action concedes, at page 5, that Davis et al. "does not teach the second generating means operates within a predetermined time interval and transmits the second fixed length data regardless of the predetermined time interval when there is no effective first fixed length packet data." Davis et al. fails to teach compulsorily transmitting fixed length packet data regardless of a predetermined time interval.

Even if Ejiri were deemed to discuss transmitting forcibly fixed packet data at the release signal timing regardless of an amount of data stored in the buffer, nothing in that patent would teach or suggest determining a transmission timing dependent on whether data is present in the buffer or not, and therefore that patent fails to teach the second generating means claimed in Claim 18.

Nothing in Davis et al. or Ejiri, whether considered separately or in any permissible combination (if any) would teach or suggest (1) generating clock reference information for use in a time reference during decoding of encoded information, (2) generating second fixed length packet data including the clock reference information to transmit the second fixed length packet data within a predetermined time interval, and (3) compulsorily transmitting the second fixed length packet data regardless of the predetermined time interval if there is no effective first fixed length packet data, as recited in Claim 18.

Accordingly, Applicant submits that Claim 18 is patentable over Davis et al. and Ejiri, whether considered separately or in any permissible combination (if any).

Independent Claims 22, 27, 28, 33, and 34 recite features similar in many relevant respects to those discussed above with respect to Claim 18 and therefore are also believed to be patentable over Davis et al. and Ejiri for at least the reasons discussed above.

The other rejected claims in this application depend from one or another of the independent claims discussed above, and, therefore, are submitted to be patentable for at least the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, individual reconsideration of the patentability of each claim on its own merits is respectfully requested.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

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